

In the Claims:

For the Examiner's convenience, all pending claims are presented below with changes shown. Please cancel claims 7-15.

1 1. (Original) A computer system comprising a microprocessor having a
2 dynamically re-configurable trace cache to provide application specific configuration of
3 the trace cache.

1 2. (Original) The computer system of claim 1 wherein the trace cache
2 comprises:
3 a tag array;
4 a data array; and
5 a next fetch address (NFA) array.

1 3. (Original) The computer system of claim 2 wherein the tag array, the data
2 array and NFA array each store one or more fetch address entries and one or more
3 temporal address entries.

1 4. (Original) The computer system of claim 3 wherein each trace stored in the
2 trace cache is assigned an index value.

1 5. (Original) The computer system of claim 4 wherein the tag array, the data
2 array and the NFA array each comprise a decoder to access a trace stored in the one or
3 more temporal address entries using an index value.

1 6. (Original) The computer system of claim 3 wherein the one or more temporal
2 address entries are generated by simulating to identify dynamic traces, the execution
3 behavior of the dynamic traces and generating an index value for each identified trace.

1 7-15. (Cancelled)

1 16. (Original) A microprocessor comprising:
2 an instruction cache to receive and store the micro-operations as cache lines;
3 a trace cache, coupled to the instruction cache, that is dynamically re-configurable
4 using profile information to provide application specific configuration of the trace cache;
5 and
6 an execution core to execute the micro-operations.

1 17. (Original) The microprocessor of claim 16 further comprising:
2 a fill unit to form micro-operations; and
3 branch prediction logic.

1 18. (Original) The microprocessor of claim 16 wherein the trace cache
2 comprises:
3 a tag array;
4 a data array; and
5 a next fetch address (NFA) array.

1 19. (Original) The microprocessor of claim 18 wherein the tag array, the data
2 array and NFA array each store one or more fetch address entries and one or more
3 temporal address entries.

1 20. (Original) The microprocessor of claim 19 wherein each trace stored in the
2 trace cache is assigned an index value.

1 21. (Original) The microprocessor of claim 20 wherein the tag array, the data
2 array and the NFA array each comprise a decoder to access a trace stored in the one or
3 more temporal address entries using an index value.

1 22. (Original) A trace cache comprising:
2 a tag array;
3 a data array; and
4 a next fetch address (NFA) array;
5 wherein the tag array, the data array and NFA array each store one or more fetch
6 address entries and one or more temporal address entries.

1 23. (Original) The microprocessor of claim 22 wherein each trace stored in the
2 trace cache is assigned an index value.

1 24. (Original) The microprocessor of claim 23 wherein the tag array, the data
2 array and the NFA array each comprise a decoder to access a trace stored in the one or
3 more temporal address entries using an index value.

1 25. (Original) The microprocessor of claim 22 wherein the one or more temporal
2 address entries are generated by simulating to identify dynamic traces, the execution
3 behavior of the dynamic traces and generating an index value for each identified trace.

1 26. (Original) A computer system comprising:
2 a microprocessor having a dynamically re-configurable trace cache to provide
3 application specific configuration of the trace cache;
4 a chipset coupled to microprocessor; and
5 a main memory coupled to the chipset.

1 27. (Original) The computer system of claim 26 wherein the trace cache
2 comprises:
3 a tag array;
4 a data array; and
5 a next fetch address (NFA) array.

1 28. (Original) The computer system of claim 27 wherein the tag array, the data
2 array and NFA array each store one or more fetch address entries and one or more
3 temporal address entries.

1 29. (Original) The computer system of claim 28 wherein each trace stored in the
2 trace cache is assigned an index value.

1 30. (Original) The computer system of claim 29 wherein the tag array, the data
2 array and the NFA array each comprise a decoder to access a trace stored in the one or
3 more temporal address entries using an index value.